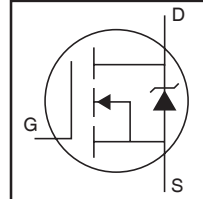


IRFB3306PbF
IRFS3306PbF
IRFSL3306PbF

HEXFET® Power MOSFET

Applications

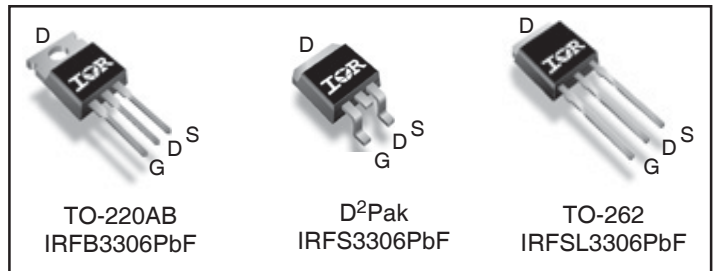
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}		60V
R_{DS(on)}	typ.	3.3mΩ
	max.	4.2mΩ
I_D		160A

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	160①	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	110①	
I _{DM}	Pulsed Drain Current ②	620	
P _D @ T _C = 25°C	Maximum Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	14	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	10lb-in (1.1N·m)	

Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	200	mJ
I _{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E _{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑥	—	0.65	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface , TO-220	0.50	—	
R _{θJA}	Junction-to-Ambient, TO-220 ⑥	—	62	
R _{θJA}	Junction-to-Ambient (PCB Mount) , D²Pak ⑥⑦	—	40	

Static @ T_J = 25°C (unless otherwise specified)

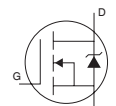
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/°C	Reference to 25°C, I _D = 5mA ^②
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	3.3	4.2	mΩ	V _{GS} = 10V, I _D = 75A ^③
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 150μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 60V, V _{GS} = 0V
		—	—	250		V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
R _G	Internal Gate Resistance	—	0.7	—	Ω	

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	230	—	—	S	V _{DS} = 50V, I _D = 75A
Q _g	Total Gate Charge	—	85	120	nC	I _D = 75A
Q _{gs}	Gate-to-Source Charge	—	20	—		V _{DS} = 30V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	26	—		V _{GS} = 10V ^⑤
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	59	—		I _D = 75A, V _{DS} = 0V, V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	15	—	ns	V _{DD} = 30V
t _r	Rise Time	—	76	—		I _D = 75A
t _{d(off)}	Turn-Off Delay Time	—	40	—		R _G = 2.7Ω
t _f	Fall Time	—	77	—		V _{GS} = 10V ^⑤
C _{iss}	Input Capacitance	—	4520	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	500	—		V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance	—	250	—		f = 1.0MHz, See Fig. 5
C _{oss eff. (ER)}	Effective Output Capacitance (Energy Related)	—	720	—		V _{GS} = 0V, V _{DS} = 0V to 48V ^⑦ , See Fig. 11
C _{oss eff. (TR)}	Effective Output Capacitance (Time Related) ^⑧	—	880	—		V _{GS} = 0V, V _{DS} = 0V to 48V ^⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	160 ^①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^②	—	—	620	A	
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 75A, V _{GS} = 0V ^⑤
t _{rr}	Reverse Recovery Time	—	31	—	ns	T _J = 25°C
		—	35	—		T _J = 125°C
Q _{rr}	Reverse Recovery Charge	—	34	—	nC	T _J = 25°C
		—	45	—		T _J = 125°C
I _{RRM}	Reverse Recovery Current	—	1.9	—	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.07mH
R_G = 25Ω, I_{AS} = 75A, V_{GS} = 10V. Part not recommended for use above this value.
- ④ I_{SD} ≤ 75A, di/dt ≤ 1400A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C_{oss eff. (TR)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ C_{oss eff. (ER)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C

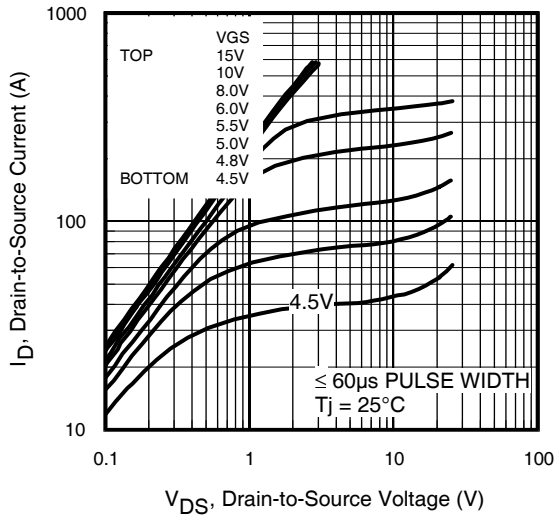


Fig 1. Typical Output Characteristics

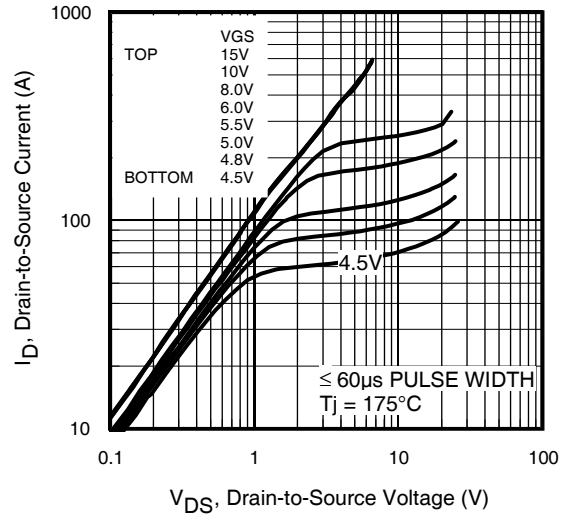


Fig 2. Typical Output Characteristics

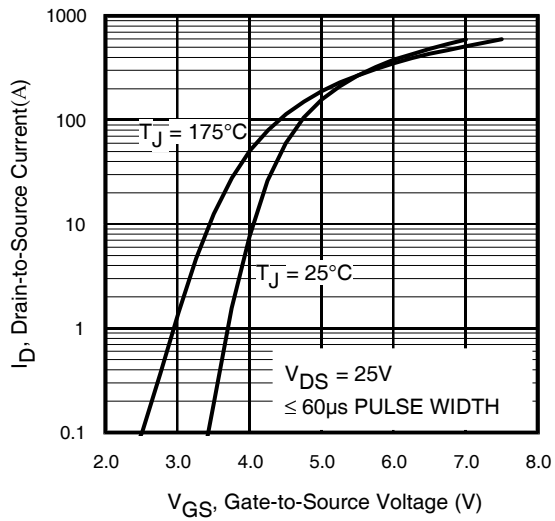


Fig 3. Typical Transfer Characteristics

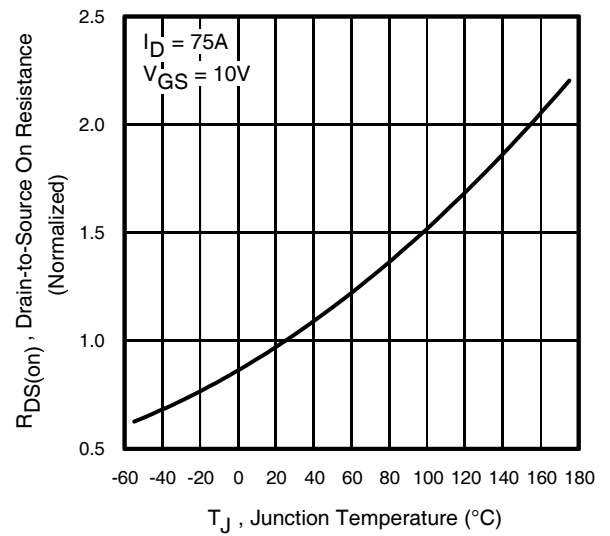


Fig 4. Normalized On-Resistance vs. Temperature

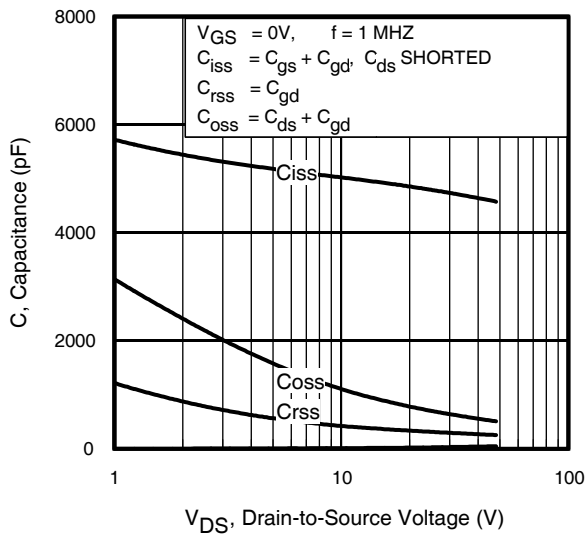


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

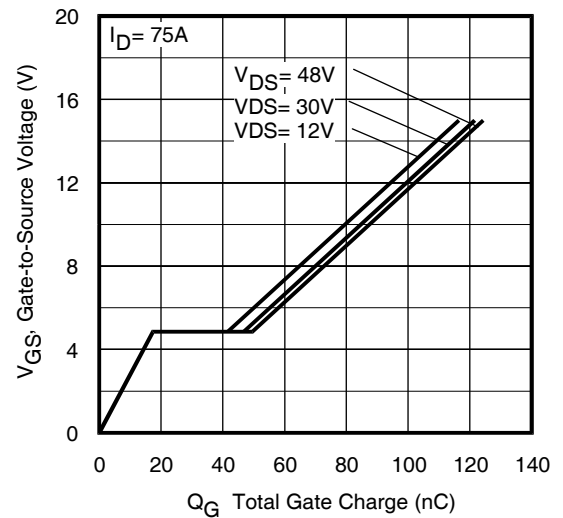


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

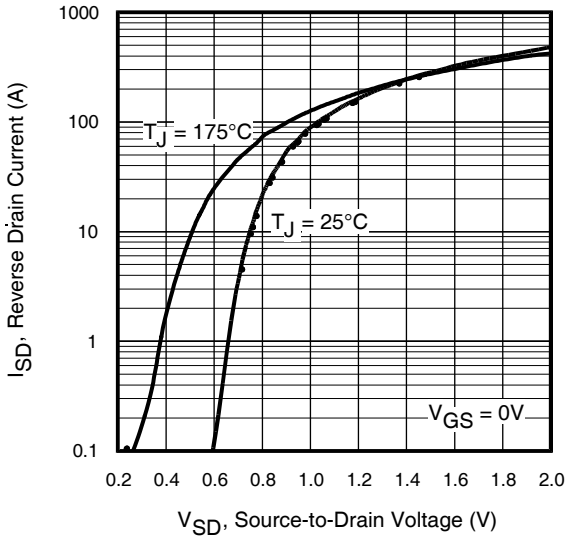


Fig 7. Typical Source-Drain Diode Forward Voltage

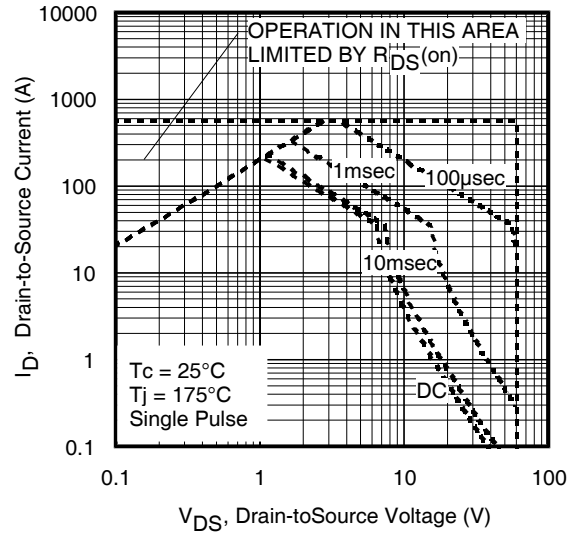


Fig 8. Maximum Safe Operating Area

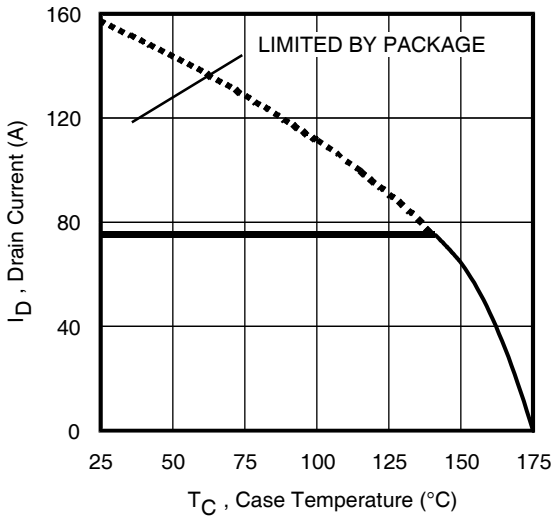


Fig 9. Maximum Drain Current vs. Case Temperature

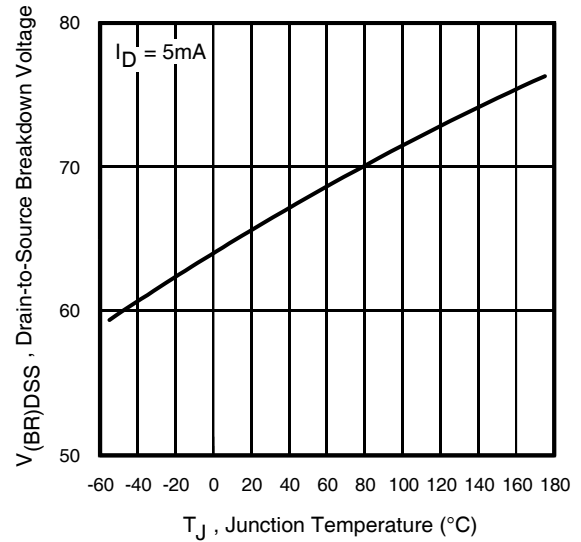


Fig 10. Drain-to-Source Breakdown Voltage

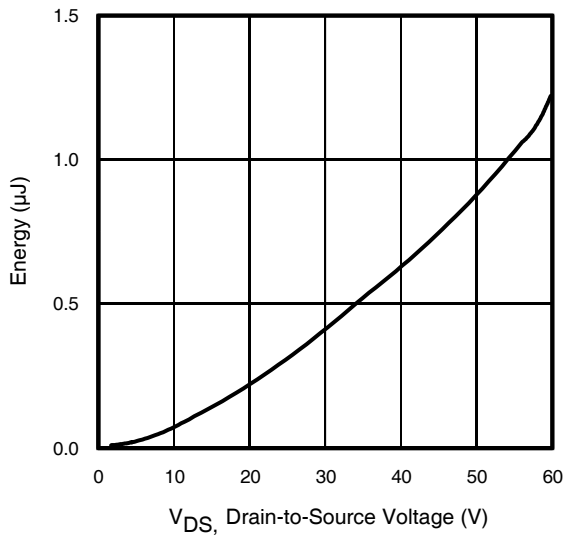


Fig 11. Typical C_{OSS} Stored Energy

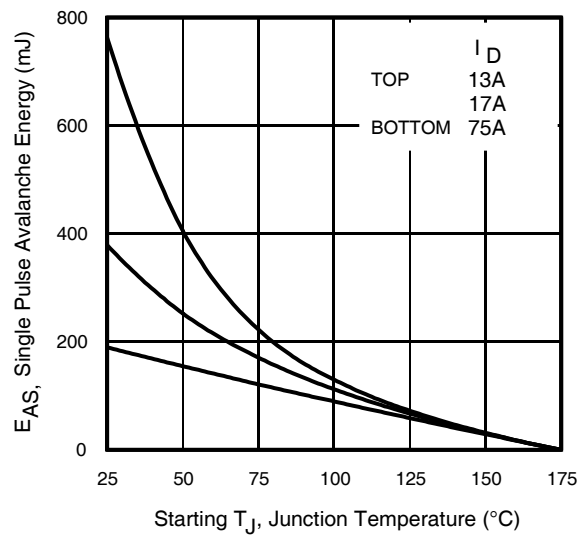


Fig 12. Maximum Avalanche Energy Vs. Drain Current

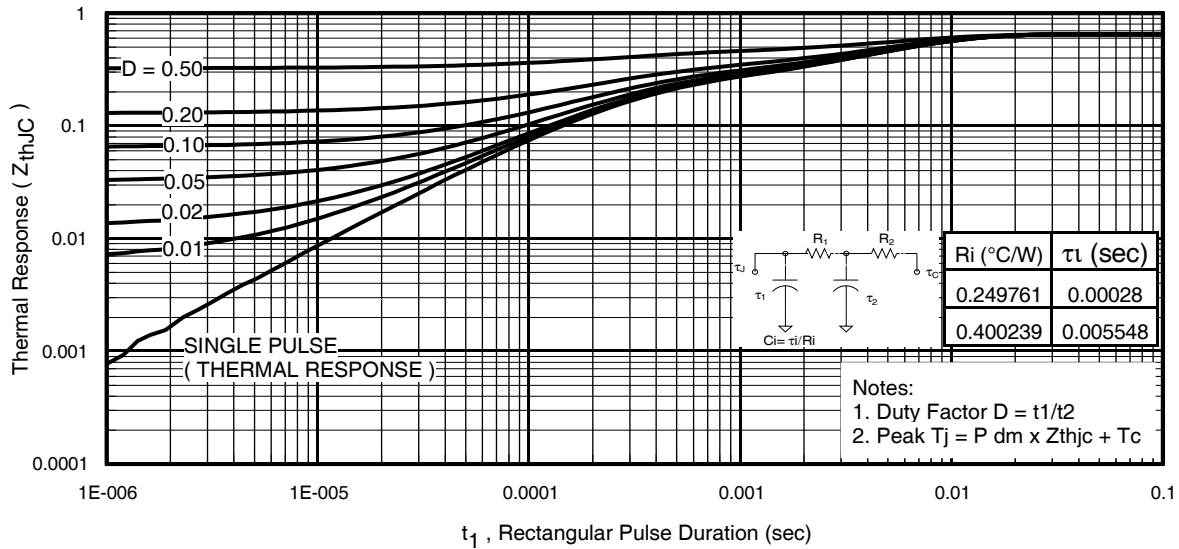


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

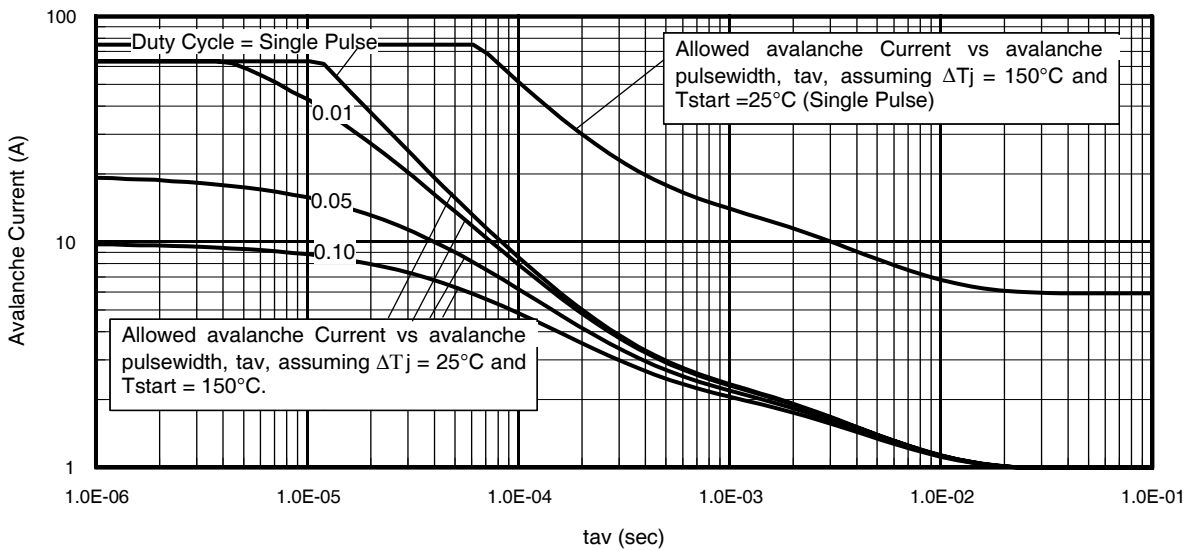
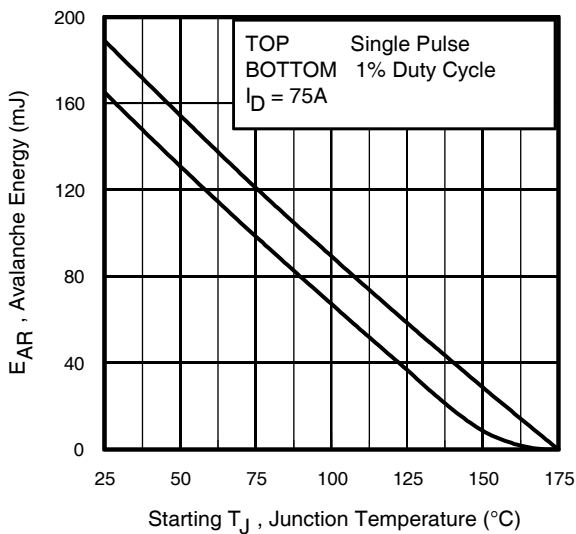


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as $25^{\circ}C$ in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

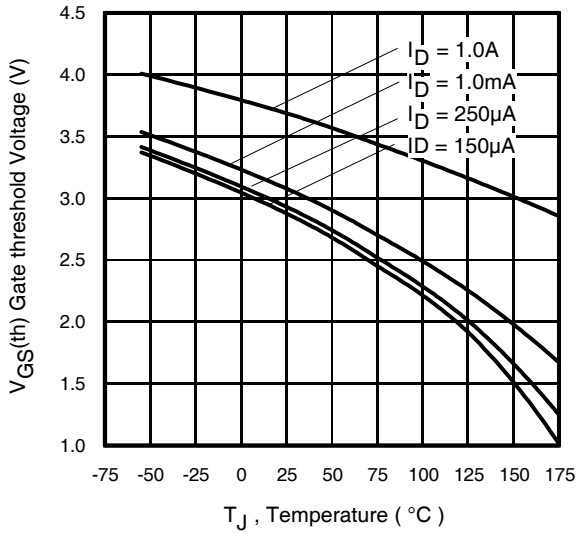


Fig 16. Threshold Voltage Vs. Temperature

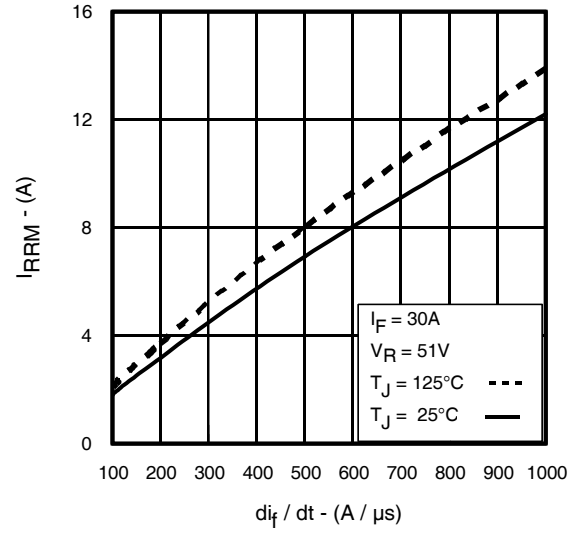


Fig. 17 - Typical Recovery Current vs. di/dt

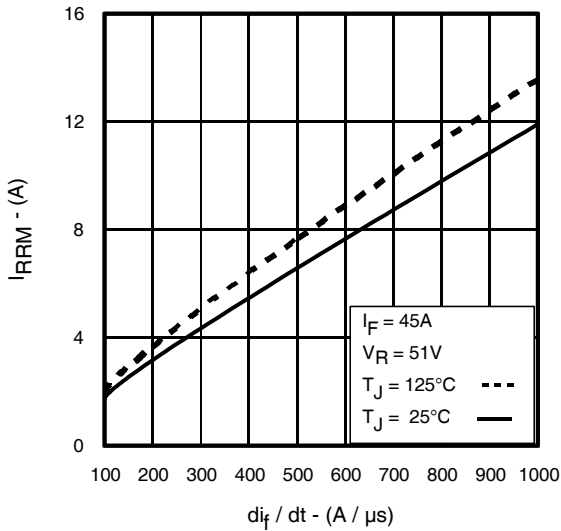


Fig. 18 - Typical Recovery Current vs. di/dt

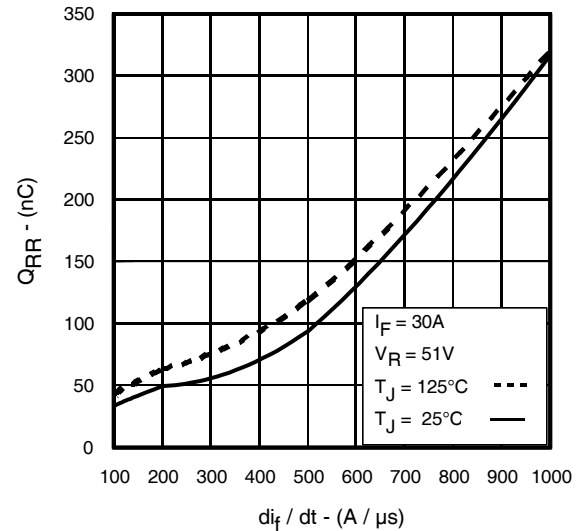


Fig. 19 - Typical Stored Charge vs. di/dt

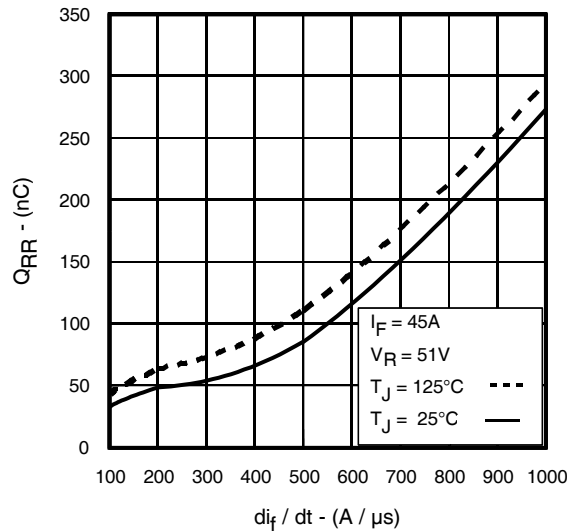
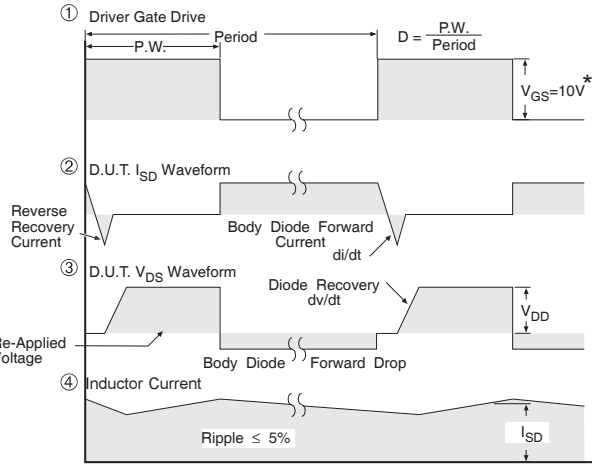


Fig. 20 - Typical Stored Charge vs. di/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

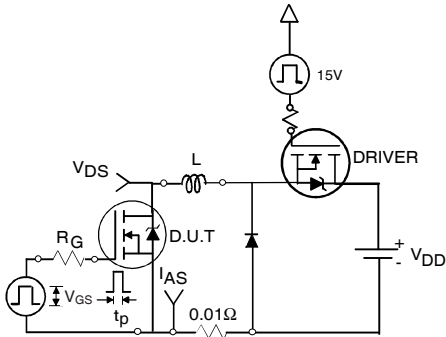


Fig 22a. Unclamped Inductive Test Circuit



Fig 22b. Unclamped Inductive Waveforms

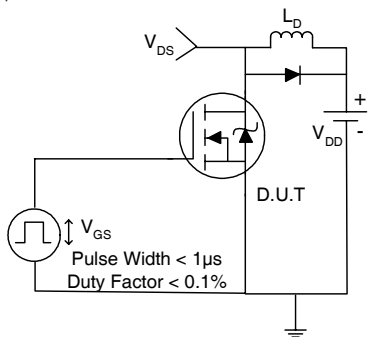


Fig 23a. Switching Time Test Circuit



Fig 23b. Switching Time Waveforms



Fig 24a. Gate Charge Test Circuit

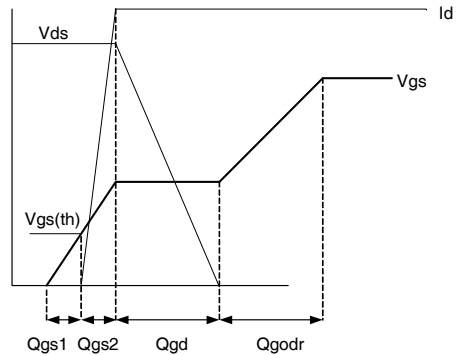
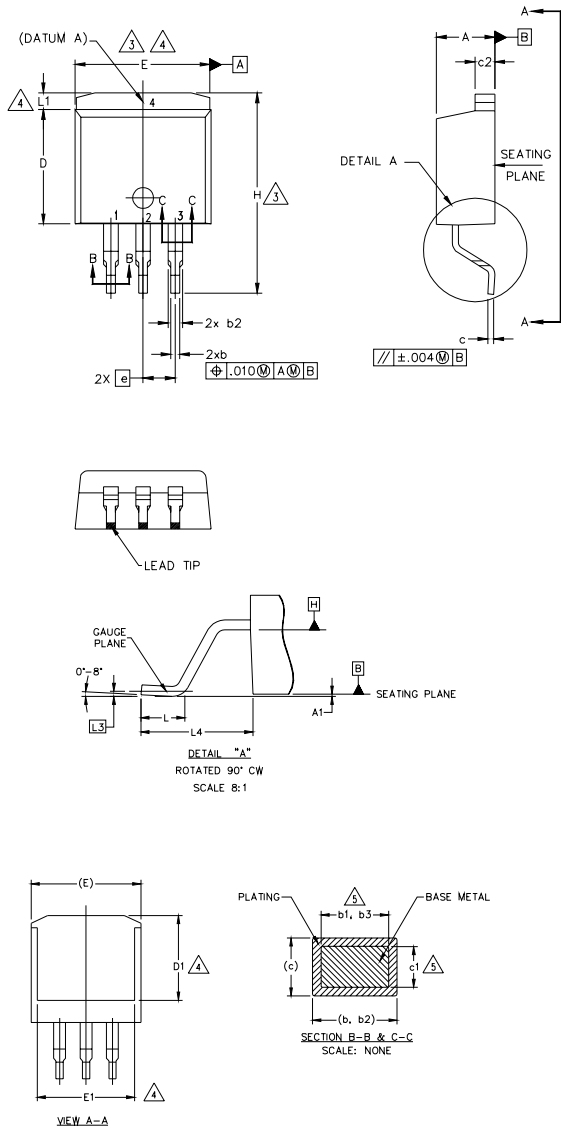


Fig 24b. Gate Charge Waveform

D²Pak Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	-	0.254	-	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	4
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

DIODES

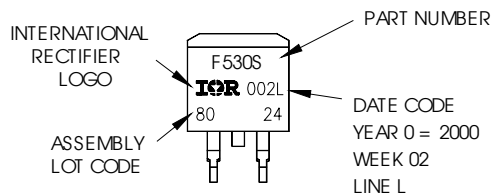
- 1.- ANODE *
- 2, 4.- CATHODE
- 3.- ANODE

* PART DEPENDENT.

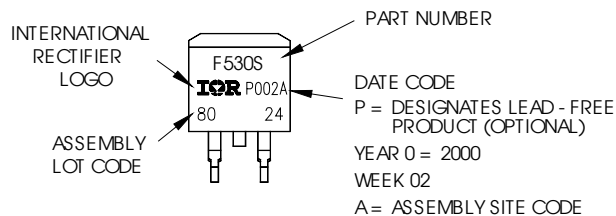
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

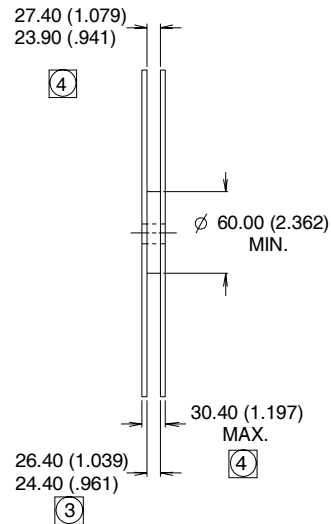
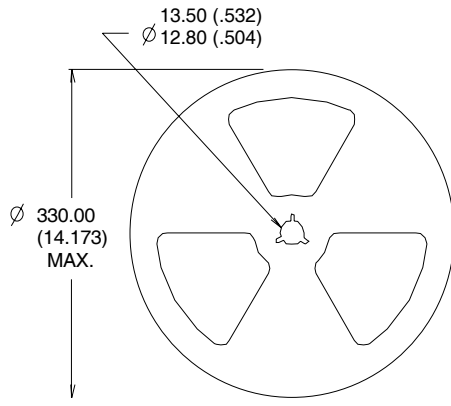
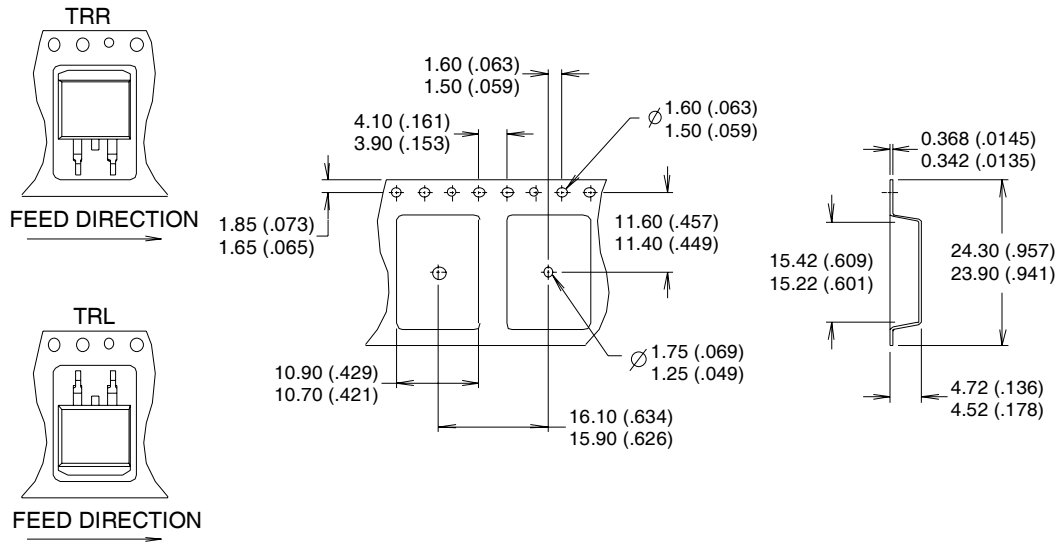
Note: "P" in assembly line position
indicates "Lead - Free"



OR



D²Pak Tape & Reel Information



- NOTES :
1. COMFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.